## REMARKS

Originally filed claims 1-4 are pending in the Application. Claims 1-3 have been examined.

Applicants thank the Examiner for the telephone conversation of February 28, 2005, in which the Applicants pointed out that the current Office Action does not address claim 4 which was originally filed with the application. Applicants submits herewith a photocopy of the filing receipt of the application dated February 13, 2004, showing that four (4) claims were originally filed. During the telephone conversation, the Examiner stated that the next office action addressing claim 4 would be issued on a non-final basis and Applicants respectfully request that the subsequent office action be non-final.

Claims 1 and 3 are rejected under 35 U.S.C. § 102(b) as being anticipated by Wu *et al.* (U.S. Patent No. 5,307,007; hereinafter "Wu"). Claims 1-3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (U.S. Patent No. 5,180,967; hereinafter "Yamazaki") in view of Wu. Applicants submit the following in traversal of the claim rejections.

Applicants respectfully submit that claim 1 is believed to be patentable because Wu fails to disclose each and every element of the claim. Claim 1 recites:

> A bias circuit having a start-up circuit, comprising:
> a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and

a start-up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

For example, Wu fails to disclose or suggest, *inter alia,* the bias circuit and the start-up circuit as recited in the claim. Specifically, Wu fails to disclose or suggest a bias circuit part using a current mirror circuit, and *for generating a constant bias voltage to an output node* from a power source voltage as applied. In the Office Action, the Examiner states that the node between NMOS transistors M1 and M3 corresponds to the claimed output node. In Wu, however, there is nothing to suggest that the node between the transistors M1 and M3 provides any sort of an output because Wu does not disclose any sort of means for detecting the voltage level at that node. Rather, the only "output" disclosed by Wu is $V_{out}$ of the voltage output regulator 40, which is entirely different from the claimed output node.

For reasons similar to those submitted for claim 1, Applicants submit that claim 3 is believed to be patentable.

Claim 2 is believed to be patentable for at least the reasons submitted for claim 1.

In addition, claim 2 is believed to be patentable because Wu fails to disclose or suggest each and every element of the claim. For example, Wu fails to disclose or suggest a resistor connected between the source of the second NMOS transistor and the grounded power source to start up circuit.

Applicants submit that claims 1 and 3 are believed to be patentable because Yamazaki in view of Wu fail to teach, suggest or provide motivation for all aspects of the claim. For

example, Yamazaki in view of Wu fail to teach, suggest or provide motivation for, *inter alia*, the claimed output node as recited in the claim.

Although the Examiner mentions nodes N11 or N12 of Yamazaki, there is nothing in Yamazaki to suggest that these nodes correspond to the claimed output node such that there is a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from a power source voltage as applied, and to a start-up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit. Rather, the nodes N11 and N12 are connected via transistors 104 and 120, to the *power source voltage* $V_{DD}$. Instead, a current $I_c$ is detected at the output. This power source voltage $V_{DD}$, is entirely different from the claimed constant bias voltage and thus, nodes N11 and N12 cannot possibly teach, suggest or provide motivation for the claimed output node.

In addition, Applicants respectfully submit that a valid motivation to combine the references has not been established. The Examiner acknowledges that Yamazaki fails to teach or suggest the claimed capacitor. *See* Office Action, page 3. The Examiner, however, alleges that Wu makes up for this acknowledged deficiency of Yamazaki by pointing out that Wu discloses capacitors C1 or C2. *See* Wu, Figs 1, 2, 4 and 6.

In particular, the Examiner, without support, concludes that "[i]t would have been obvious to one of ordinary skill in the art at the time of the invention to replace the start up circuits 118 & 120 with a start up capacitor as taught by Wu et al. for the benefit of reducing component count and static current consumption." Applicants respectfully disagree

with the Examiner because there is nothing to suggest that one skilled in the art would believe that there is a reasonable expectation of success in the combination of Yamazaki and Wu suggested by the Examiner.

For at least the above reasons, Applicants believe that claim 1 is believed to be patentable over Yamazaki and Wu.

For reasons similar to those submitted for claim 1, claim 3 is believed to be patentable.

Consequently, claim 2, which depends from claim 1, is believed to be patentable over Yamazaki and Wu for at least the reasons set forth above for claim 1.

Claim 4, which depends from claim 3, is believed to be patentable for at least the reasons submitted for claim 3.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

Seok-Won Stuart Lee*
*Granted limited recognition under 37 C.F.R. § 11.9(b), as shown in a copy of the same filed on May 2, 2005, at the U.S.P.T.O.

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: May 2, 2005

**BEFORE THE OFFICE OF ENROLLMENT AND DISCIPLINE**
**UNITED STATES PATENT AND TRADEMARK OFFICE**

## LIMITED RECOGNITION UNDER 37 CFR § 11.9(b)

Seok-Won Lee is hereby given limited recognition under 37 CFR § 11.9(b) as an employee of the Sughrue Mion, PLLC law firm to prepare and prosecute patent applications wherein the patent applicant is the client of the Sughrue Mion, PLLC law firm, and the attorney or agent of record in the applications is a registered practitioner who is a member of the Sughrue Mion, PLLC law firm. This limited recognition shall expire on the date appearing below, or when whichever of the following events first occurs prior to the date appearing below: (i) Seok-Won Lee ceases to lawfully reside in the United States, (ii) Seok-Won Lee's employment with the Sughrue Mion, PLLC law firm ceases or is terminated, or (iii) Seok-Won Lee ceases to remain or reside in the United States on an H1B visa.

This document constitutes proof of such recognition. The original of this document is on file in the Office of Enrollment and Discipline of the United States Patent and Trademark Office.

**Expires: May 29, 2005**

Harry I. Moatz
Director of Enrollment and Discipline

67

**REQUEST FOR EARLY NOTIFICATION OF SERIAL NUMBER**


Inventor(s): Jae-jun MOON, Jeong-won LEE, and Jung-eun LEE

Title: BIAS CIRCUIT HAVING START-UP CIRCUIT

Atty Doc. #: **Q77183** Client: NAWOO PATENT & LAW FIRM

Filing Date: **February 13, 2004** # Pgs. Spec/Abst: 18/1 #Claims: 4

# Dwg. Sheets: 11 Decl YES (4 pgs.) Prelim Amdt NO

IDS/Prior Art: NO Pr Doc: YES (1) Asgmt: YES Fee: $770/$40
& PTO 1595 form

☑ Check Attached ☐ Charge to Deposit # 19-4880 Atty/Sec: DM/lck

SERIAL NO.: CONF NO.: